REMARKS

The following remarks are made in response to the Office Action mailed December 29, 2004, in which claims 1-17 and 29-33 were rejected. With this Response, claims 13-17 and 33 have been canceled from the application. Claims 1-12 and 18-32 remain pending in the application, with claims 18-28 previously withdrawn from consideration.

Claim Rejections under 35 U.S.C. § 102

Claims 1-3 and 8-10 stand rejected under 35 U.S.C. §102(e) as being anticipated by Childress et al. (U.S. Patent Application Publication No. 2003/0231437).

Regarding claim 1, the Examiner asserts Childress et al. discloses a memory wafer comprising a first surface (of substrate 9, 109 in Figures 1 and 2) having memory chips disposed thereon, the memory chips defining an exterior face (150 of Figure 2) of the memory wafer. The Examiner further alleges Childress et al. discloses a second surface (of substrate 9, 109) opposite the exterior face 150, and a top magnetically permeable shield layer on top surface 150 (not shown).

The Examiner's rejection is respectfully traversed. Under 35 U.S.C. §102, the cited reference must show each and every feature of the claimed invention. Extension of or speculation as to the cited teaching is permitted only when *necessarily present* in the disclosed apparatus or method. In other words, if a particular feature is not specifically disclosed it can only be relied upon under 35 U.S.C. §102 if and only if such feature is necessarily present in the disclosed apparatus or method. See, *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)("A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference"), and *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) ("The identical invention must be shown in as complete detail as is contained in the ... claim").

As set forth in the application, claim 1 claims a memory wafer comprising a first surface having memory chips disposed thereon, the memory chips defining an exterior face of the memory wafer, a second surface opposite the exterior face, and a magnetically permeable

shield layer extending over at least one of the exterior face and the second surface of the memory wafer.

Childress et al. fails to anticipate the subject matter of claim 1 for at least the reason that Childress et al. fails to disclose a memory wafer having memory chips disposed thereon. Rather, Childress et al. discloses a **single** magneto-resistive device on a substrate, and in particular a **single** magnetic tunnel junction. The entire disclosure of Childress et al. relates to a **single** magneto-resistive element, and does not teach or suggest that more than one magneto-resistive element be disposed on the substrate. In fact, Childress et al. references the device as a single "memory cell", which is distinctly different from a memory wafer having memory chips disposed thereon. The specification of the present application clearly describes, in paragraphs 25 and 26, that a memory wafer 100 includes a plurality of separable memory chips 110, each of the separable memory chips include multiple memory arrays, and each of the memory arrays have multiple memory cells. Clearly, the single memory cell disclosed by Childress et al., cannot be said to be the same as the memory chips and memory wafer in claim 1. Further, more than one magnetic tunnel junction are not necessarily present in Childress et al., as the read head of Childress et al. only requires a single magneto-restive device.

Claim 1 further sets forth that the memory wafer includes "a magnetically permeable shield layer extending over at least one of the exterior face and second surface **of the memory wafer**". As described above, Childress et al. does not disclose a memory wafer having memory chips disposed thereon. Accordingly, Childress et al. does not disclose a magnetically permeable shield layer extending over at least one of the exterior face and second surface of the memory wafer. Further, such a shield layer is not necessarily present in Childress et al., as the read head of Childress et al. only requires a single magnetorestive device.

For at least the reasons provided above, the claimed memory wafer having memory chips disposed thereon is not anticipated by Childress et al., and the claimed elements are not *necessarily present* in the reference. Accordingly, claim 1 is in allowable condition, and withdrawal of the rejection of claim 1 under 35 U.S.C. §102(e) is respectfully requested.

Claims 2-3 and 8-10 depend, either directly or indirectly, from independent claim 1, which is in allowable condition for at least the reasons set forth above. Accordingly,

dependent claims 2-3 and 8-10 are also in allowable condition, and withdrawal of the rejection under 35 U.S.C. §102(e) is respectfully requested.

Claims 13, 14, and 17 stand rejected under 35 U.S.C. §102(e) as being anticipated by Rizzo et al. (U.S. Patent Application Publication No. 2004/0000415).

With this Amendment, claims 13, 14, and 17 have been cancelled from the application.

Claim Rejections under 35 U.S.C. § 103

Claims 4-7 and 10-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Childress et al. (U.S. Patent Application Publication No. 2003/0231437) in view of Rizzo et al. (U.S. Patent Application Publication No. 2004/0000415).

Claims 4-7 and 10-12 each depend, either directly or indirectly, from independent claim 1 which is in allowable condition for at least the reasons set forth above. As described above, Childress et al. fails to anticipate or suggest the elements of independent claim 1. Rizzo et al. does not remedy the deficiencies of Childress et al., as Rizzo et al. also fails to disclose or suggest a memory wafer having memory chips disposed thereon, and further fails to disclose or suggest a magnetically permeable shield layer extending over at least one of the exterior face and the second surface of the memory wafer. Accordingly, the combination of Childress et al. and Rizzo et al. also necessarily fails to disclose the elements of the claims depending from independent claim 1. For at least these reasons, dependent claims 4- 7 and 10-12 are not obvious over Childress et al. in view of Rizzo et al. Accordingly, withdrawal of the rejection of claims 4-7 and 10-12 under 35 U.S.C. §103(a) is respectfully requested.

Claims 15 and 16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Rizzo et al. (U.S. Patent Application Publication No. 2004/0000415) in view of Tuttle et al. (U.S. Patent Application Publication No. 2003/01322494).

With this Amendment, claims 15 and 16 have been cancelled from the application.

Claims 29 and 30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over

Childress et al. (U.S. Patent Application Publication No. 2003/0231437) in view of Tuttle et al. (U.S. Patent Application Publication No. 2003/01322494).

Regarding claim 29, Childress et al. is alleged to disclose a memory wafer comprising a first surface (of substrate 9, 109 in Figures 1 and 2) having memory chips disposed thereon, the memory chips defining an exterior face 150 of the memory wafer. Childress et al. is further alleged to disclose a second surface (of substrate 9, 109) opposite the exterior face 150, and a top magnetically permeable shield layer on top of surface 150 (not shown).

Childress et al. is acknowledged as failing to explicitly show means for protecting the memory cells from stray magnetic fields. However, Tuttle et al. is cited as showing the use of magnetically permeable foils 26 and 28 as shields from stray magnetic fields. The Examiner alleges the magnetically permeable layers of the Childress et al. device are identical to the shields of Tuttle et al., and therefore alleges that the magnetically permeable layers of Childress et al. can be used as means for protecting from external magnetic fields.

The Examiner's rejection of independent claim 29 is respectfully traversed. Independent claim 29 is directed to a memory wafer including a first surface having memory chips disposed thereon. As discussed above with respect to independent claim 1, Childress et al. discloses only a single memory cell. Childress et al. fails to disclose an array of memory cells, a memory chip comprised of an array of memory cells, or a memory wafer having a plurality of memory chips, as described and claimed in the present application. Further, the claimed elements are not *necessarily present* in Childress et al. Tuttle et al. fails to remedy the deficiencies of Childress et al., as Tuttle et al. also fails to disclose a memory wafer having memory chips disposed thereon. Accordingly, the subject matter of independent claim 29 is not obvious in view of the combination of Childress et al. and Tuttle et al. for at least this reason. Accordingly, withdrawal of the rejection of independent claim 29 under 35 U.S.C. §103(a) is respectfully requested.

Dependent claim 30 depends directly from independent claim 29, which is allowable for at least the reason set forth above. Accordingly, dependent claim 30 is also in allowable condition for at least the same reason, and withdrawal of the rejection of dependent claim 30 under 35 U.S.C. §103(a) is respectfully requested.

Claims 31 and 32 are rejected under 35 U.S.C. §103(a) as being unpatentable over Childress et al. (U.S. Patent Application Publication No. 2003/0231437) in view of Tuttle et al. (U.S. Patent Application Publication No. 2003/01322494) and further in view of Rizzo et al. (U.S. Patent Application Publication No. 2004/0000415).

Dependent claims 31 and 32 depend from independent claim 29, which is in allowable condition for at least the reasons discussed above. Rizzo et al. fails to overcome the deficiencies of Childress et al. and Tuttle et al., as Rizzo et al. also fails to disclose a memory wafer having memory chips disposed thereon. According, dependent claims 31 and 32 are also in allowable condition, and withdrawal of the under 35 U.S.C. §103(a) is respectfully requested.

Claim 33 is rejected under 35 U.S.C. §103(a) as being unpatentable over Rizzo et al. (U.S. Patent Application Publication No. 2004/0000415).

With this Amendment, claim 33 has been cancelled from the application.

CONCLUSION

For at least the reasons discussed above, claims 1-12 and 29-32 are in allowable condition and notice to that effect is respectfully requested.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to either Matthew B. McNutt at Telephone No. (512) 231-0531, Facsimile No. (512) 231-0540, or Phil Lyren at Telephone No. (281) 514-8236, Facsimile No. (281) 514-8332. In addition, all correspondence should continue to be directed to the following address:

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 21st day of February, 2005.

By _____
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